

Crystal Oscillator 40 MHz

1 Features

- Suitable for RF Applications
- Nominal frequency 40 MHz
- Parallel resonance
- Low phase noise
- 0.18 μm TSMC technology
- Bypass mode (external clock)
- Input signal level for Bypass mode 1Vpp
- Power down (standby) mode
- 1.8 V Single supply
- Constant gm circuit stabilizes the amplifier over process and temperature variations

2 General Description

The crystal oscillator (XO) is intended to run at a frequency of 40 MHz. The crystal oscillates in parallel resonance. Normally the external capacitors C106, C107 (connected from Xtal1 and from Xtal2 to ground) determine frequency centering. The XO's

phase noise is a predominant contributor to the overall synthesizer's phase noise; so the crystal has to be carefully chosen, compliant to the given specification. The signal from the oscillator is buffered. Possible applications for this oscillator are a reference for digital clocks in the RF part and in the associated digital baseband. It is recommended to use a clock buffer which supplies two digital outputs (CPOUT and CLKOUT); the first stage of the clock buffer can be biased with a constant gm circuit.

A second sinusoidal buffer can be used and connected via ac-coupling to the XO. The operating point of this buffer is centered and independent of temperature and process variations. The sinusoidal output of this buffer is REFOUT. The harmonics of this signal are satisfactory attenuated, thus, this signal is suitable to use as an external clock reference.

Chip size for XO core and clock buffer is 140 μm x 90 μm .

Chip size for sinusoidal buffer is 175 μm x 55 μm .

3 Block Diagram

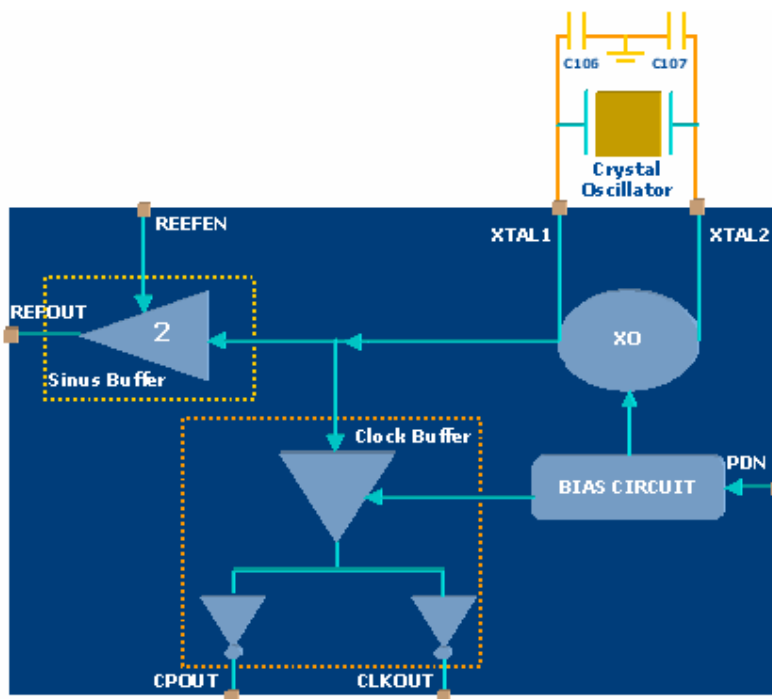


Figure 1: Functional Block Diagram

4 Signal Description

Signal Name	Direction	Size	Description
vssl	Input	1	Analog ground
vddl	Input	1	Analog supply voltage
vsssub	Input	1	Ground connection for the substrate Guardring
xtal1, xtal2	In-Out	2	External crystal Pins
pdn		1	General power down If this signal is set to low the circuitry is switched off
refout	Output	1	Sinusoidal output of the sinusoidal buffer
refen	Input	1	Enable sinusoidal output.
cpout	Output	1	First digital clock signal output of the clock buffer
Clkout	Output	1	Second digital clock signal output of the clock buffer

Table 1: Crystal Oscillator Signal Description

4.1 Settings

Signal pdn (pdn=high) is used to switch off the XO circuitry, which comprises the biasing circuit, XO core and clock buffer. If the XO circuitry is being bypassed, the sinusoidal buffer can be disabled (setting refen=0) to save power.

5 Symbol

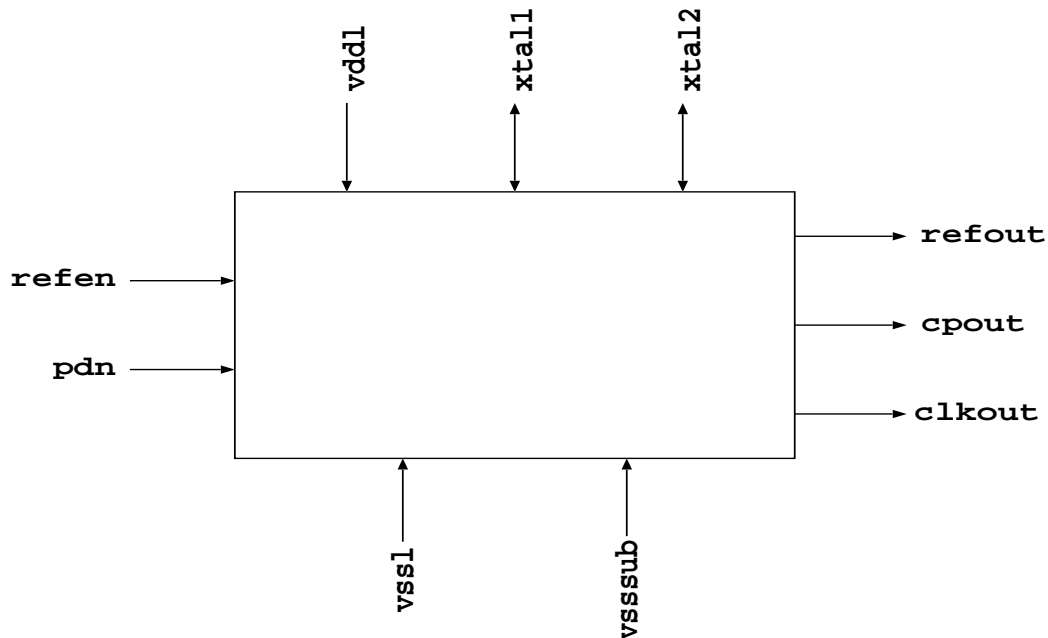


Figure 2: Oscillator Symbol

6 Electrical Characteristics

6.1 Operating Conditions

Parameter	Min	Typ	Max	Unit
Nominal Frequency		40		MHz
Temperature Range	-30	27	85	°C
Supply Range	1.8-10%	1,8	1.8+10%	V
Current consumption			2	mA

6.2 AC Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Tolerance	10pF total load capacitance			+/-10	ppm
Frequency Accuracy on REFOUT	Sinusoidal Buffer on and off				
Versus VDD (pushing)	Vsupply from 1.2V to 2.2V ZLoad=50Ω			Figure 2a,2b	ppm
Versus Load (pulling)	C106,C107 15pF to 20pF(*)			Figure 2a,2b +/-15	ppm
Versus Temp	Vsupply=1.8V, Zload=2kΩ/10pF				ppm
Output Level					
REFOUT	Cload=10pF Load=50Ω		1.56 0.4		Vpp Vpp
CPOUT	Zload=100fF	0.3		Vsupply- 0.3	V
CLKOUT	Zload=100fF	0.3		Vsupply- 0.3	V
Output duty cycle					
CPOUT	Xtal1 node>100mV	30		70	%
CLKOUT	Xtal1 node>100mV	30		70	%
CPOUT	Xtal1 node>200mV	40		60	%
CLKOUT	Xtal1 node>200mV	40		60	%
Input Signal level	Bypass mode	1			Vpp
Rise time for CPOUT and CLKOUT	From 5% to 95% of the step Load=50fF Load=100fF	80 125		140 212	psec psec
Phase noise on REFOUT	Vsupply=1.9V, XO_EN=high, PDN=0		Figure 3		dBm
Turn on time REFOUT	Vsupply=1.9V; XO_EN=high, 50Ω load		Figure 4	5	ms
Spectrum	Vsupply=1.9V, 50Ω		Figure 5		
HD2			-37		dB
HD3			-34		dB

(*) C106 and C107 are external capacitances (connected to XTAL1 and XTAL2) required for the parallel resonance made of operation.

XO frequency accuracy vs. VDDXO supply voltage

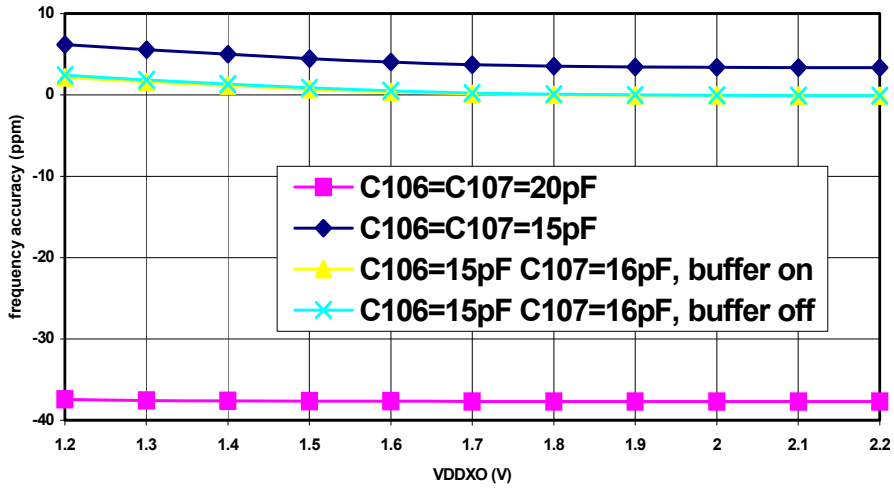


Figure 2a: XO Frequency Accuracy vs. Supply Voltage

XO frequency accuracy vs. VDDXO supply voltage

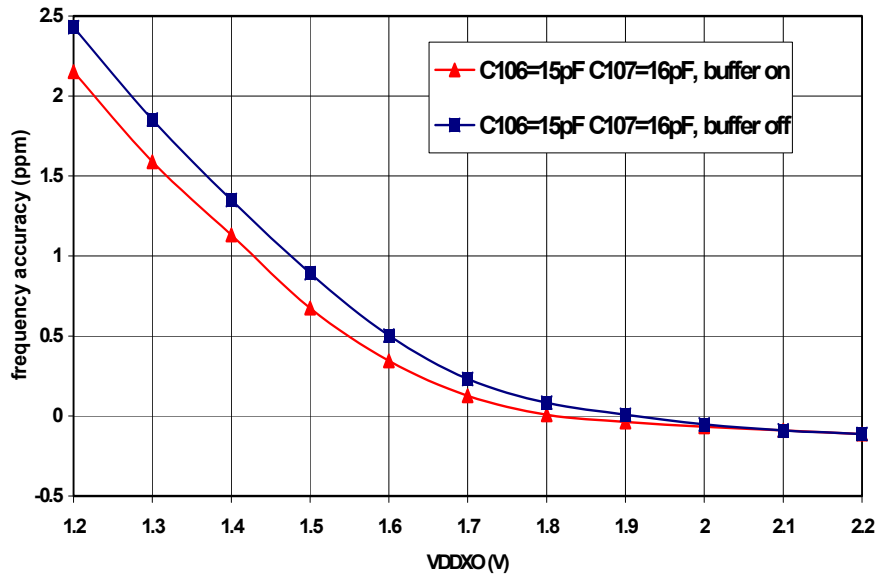


Figure 2b: XO Frequency Accuracy vs. Supply Voltage - ZOOM

Red = Floor Noise PN9000
White = XO phase noise

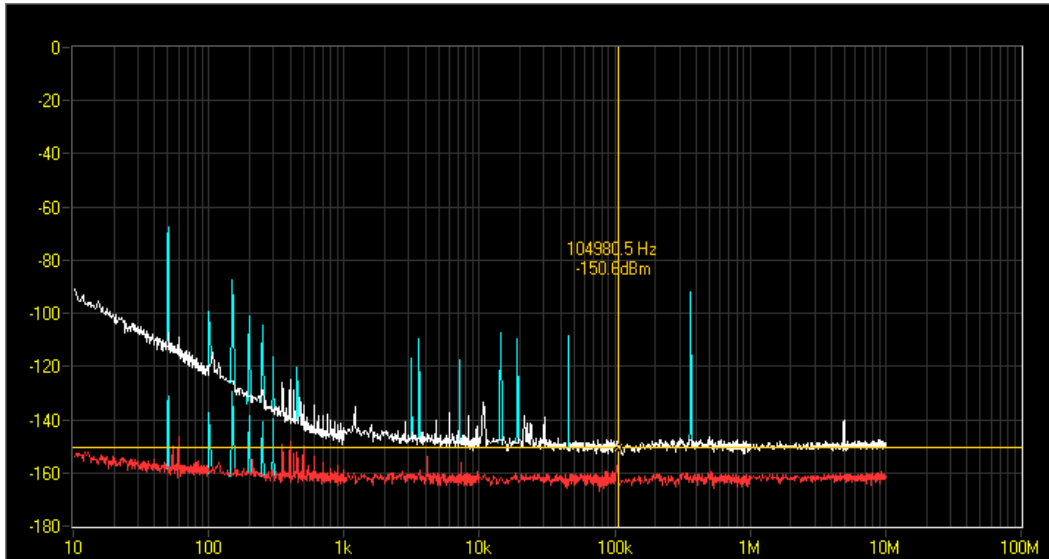


Figure 3: Phase Noise

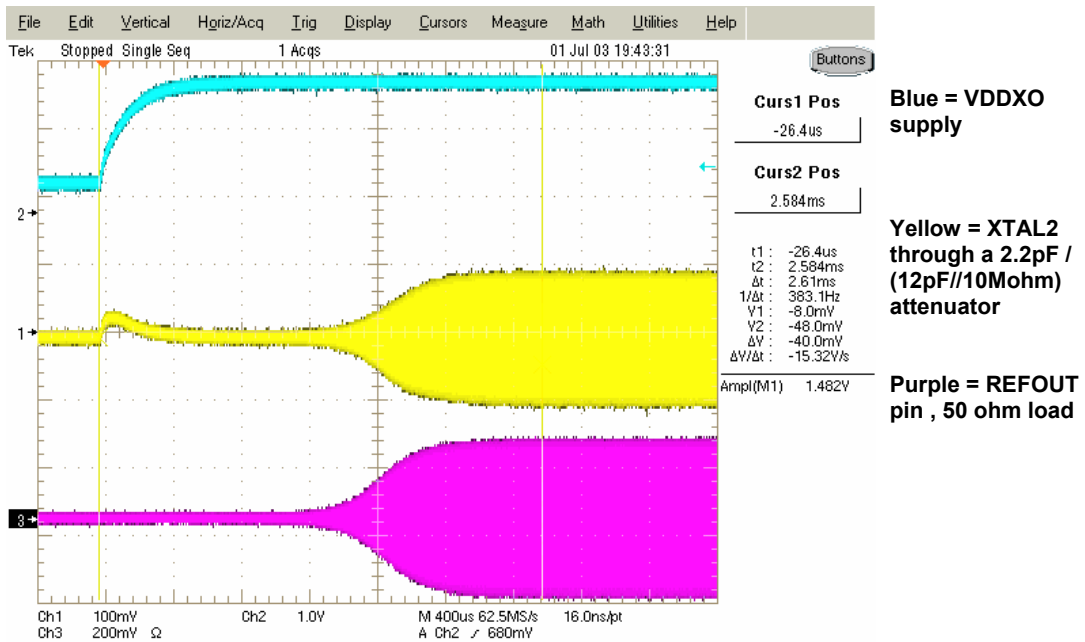


Figure 4: Turn on Time

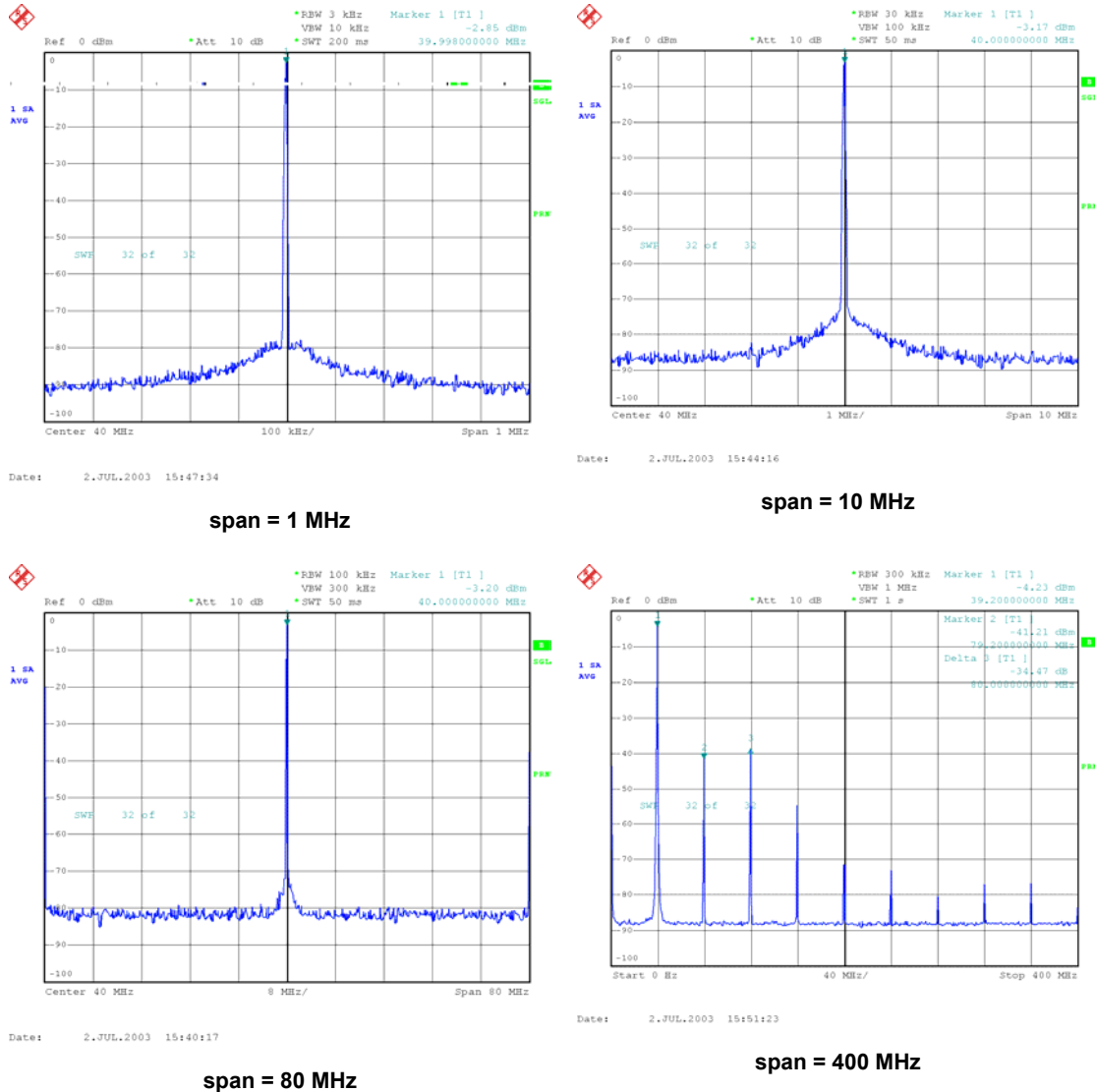


Figure 5: REFOUT Spectrum

6.3 Definitions of Specifications

6.3.1 Frequency Accuracy and Stability

We can define two types of frequency specifications which depend on the way the circuit is connected externally:

- the frequency accuracy
- the frequency stability.

The accuracy is the oscillator's capacity to run at a specific frequency. Generally, it demands that the oscillator characteristics (principally the load capacitance) are matched according to the crystal manufacture specifications.

In this case the frequency accuracy is defined as:

$$Accuracy (ppm) = \frac{10^6 \cdot (Frequency\ measured - 40\ MHz)}{40\ MHz}$$

The stability is the oscillator's capacity to keep this frequency stable.

6.3.2 Turn on Time

This is the necessary start time to have a clock signal with a duty cycle inside specification (40-60%).

6.3.3 Phase Noise

As with other analogue circuits, oscillators are susceptible to noise. Noise injected into an oscillator by its constituent devices or by external means may

influence both frequency and the amplitude of the output signal.

Here only the random deviation of the frequency is considered. For a nominal periodic sinusoidal signal, we can write:

$$x(t) = A \cdot \cos(\omega_c \cdot t + \phi(t))$$

where ω_c is the ideal sinusoidal oscillator pulse and $\phi(t)$ is called "phase noise". The phase noise is characterized in the frequency domain.

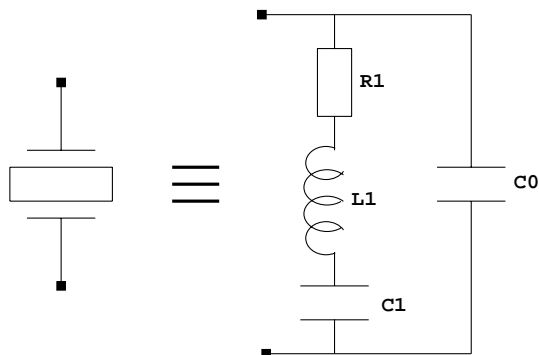
6.3.4 Duty Cycle

The switch point in the digital clock buffer would move due to process and temperature variations. Therefore the first stage of clock buffer is biased, with constant gm circuit. The duty cycle of the output clock was measured as the time difference of two successive crossing of $V_{supply}/2$.

7 Theory of Operation

Crystal oscillators use an external crystal to generate clock signals for designs that require high stability at a precise frequency.

The mechanical impedance of a crystal for one particular series resonant frequency k can be electrically modeled by a series RLC resonant circuit.



The parasitic capacitance of the crystal's electrodes and the package are modeled by the capacitor C_0 . (C106 and C107)

Using the electrical model, the main parameters of a crystal can be extracted:

Resonant Frequency:

$$f_x = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot L_1}}$$

Quality factor Q_x :

$$Q_x = 2 \cdot \pi \cdot f_x = \frac{1}{\sqrt{C_1 \cdot L_1}} = \frac{2 \cdot \pi \cdot f_x \cdot f_x}{f_x} = \frac{1}{2 \cdot \pi \cdot f_x \cdot C_1 \cdot L_1}$$

Mechanical Impedance Z_x :

$$Z_x = R_1 + j \cdot \frac{1}{2 \cdot \pi \cdot f_x \cdot C_1} \cdot \left(\frac{f}{f_x} - \frac{f_x}{f} \right)$$

The critical parameter for frequency stability of any oscillation is the frequency pulling P , which is defined as the relative drift of the current frequency f from the resonant frequency f_x :

Frequency Pulling P_x :

$$P_x = \frac{f - f_x}{f_x}$$

so:

$$Z_x = R_1 + j \cdot \frac{2 \cdot P_x}{2 \cdot \pi \cdot f_x \cdot C_1}$$

Because a crystal has natural losses, which are expressed by the resistance R_1 in the model, it is impossible for the crystal itself to build up an oscillation. An oscillator circuit has to be used to apply an impedance Z_c to the crystal that compensates R_1 .

At turn on, when noise is generated, $x(t) = A \cdot \cos(\omega_c \cdot t + \phi_n(t))$ is generated by the device and then amplified. This noise is fed back positively through a "frequency separation" (crystal) to the input where it is amplified again and so on.

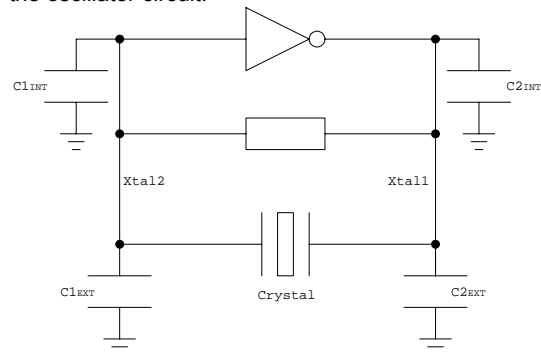
The critical condition for oscillation can be achieved by comparing the real components of the impedance of crystal and oscillator (oscillator includes C_0):

$$-\text{Real}[Z_x] = R_1$$

As soon as $-\text{Real}[Z_c]$ is larger than R_1 , an oscillation builds up exponentially in the crystal, until its amplitude is limited by non-linearity or additional regulation circuitry. The time constant T for oscillation to build up depends on both the crystal and the oscillator impedance:

$$T = \frac{-L_1}{(\text{Real}[Z_x] + R_1)} = \frac{1}{(\omega^2 \cdot C_1 \cdot (\text{Real}[Z_x] + R_1))}$$

The following figure shows the implementation of the oscillator circuit.



The capacitors C1_{INT} and C2_{INT} are implemented in the cells on-chip. The bias resistor R_F is an internal resistance required to force the transistor into its active mode. Its value should be very high to avoid degrading the frequency stability and increasing the current.

In order to have the minimum variation on the output frequency ($\Delta f/f$), the parasitic capacitance on the PCB (Xtal1-GND, and Xtal2-GND) should be estimated or measured. If the parasitics are significantly less than what is needed, external I capacitances (C1_{EXT} and C2_{EXT}) should be added in the feedback path of oscillator (in parallel with the crystal).

8 Application Note

In bypass mode the circuit has to operate without the quartz crystal, only stimulated with an external clock signal. In this case the sinusoidal buffer can be disabled to save power.

In order to reach the frequency accuracy that we have specified, it's recommended to use external capacitors C106=15pF and C107=16pF and the NDK NX3225 DI quartz crystal.

9 Deliverables

As part of the License Agreement the components listed below will be delivered:

- Schematic
- Layout
- Datasheet

10 Contact

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