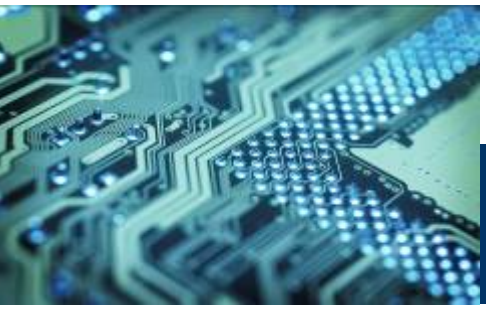

1.8 V / 3.3 V LVDS Transceiver

1 Features

- Up to 250 Mb/s (250 MHz clock) switching rate
- Multi Voltage/Multi Current capabilities
- Driver outputs in high impedance with power down
- Connection enabled independently
- Two modes:
  - o High current mode: +/-400 mV differential swing (4 mA per connection)
  - o Low current mode: +/-200 mV differential swing (2 mA per connection)
- +/-100 mV receiver threshold
- Fail safe mode: the receiver output is maintained to low voltage when inputs are not driven (open or shorted)
- PCB lines up to 100 mm long in low current mode
- Twisted pair connection up to 1 m long, using CAT5e cable
- 3.3 V supply +/-10% and 1.8 V supply +/-10%

2 Technology

TSMC 0.18um CMOS Process

3 General Description

Wipro-NewLogic's LVDS interface (driver & receiver) is based on the IEEE standard. The line driver and receiver are designed to support data rates in excess of 250 Mb/s (250 MHz clock).

Two modes of operation are available: high and low current modes:

1. High Current Mode
2. Low Current Mode

LVDS uses a constant current mode driver. Transmission line is terminated by an external load resistor (which value is between 90 and 110 Ω). When the driver is disconnected (tri-state mode or powered off), the receiver output is maintained to low voltage (fail-safe mode), preventing from switching due to the noise on the line.

4 Block Diagram

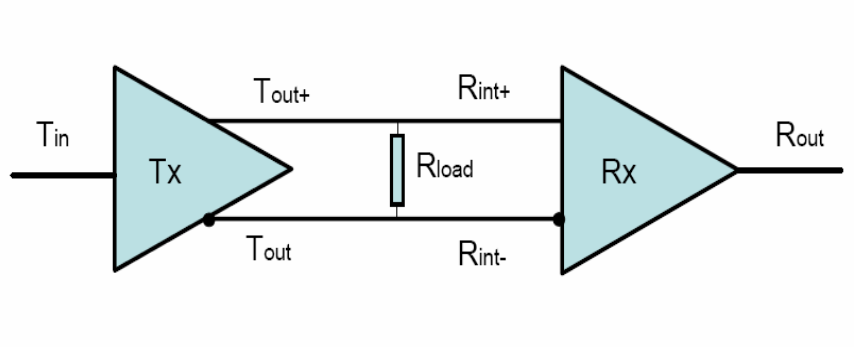

Figure 1: Functional Block Diagram

5 Deliverables

- GDSII
- Basic AHDL Simulation models
- Datasheet
- Application Note and Test Guidelines

6 Applications

- RF applications including Bluetooth, WLAN
- Wired applications – Serial ATA, Spacewire.
- Video, Imaging applications – digital camera interface, LCD display interface

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