

10 GHz Frequency Synthesizer

1 Features

- 10 GHz Fractional-N fully integrated frequency synthesizer
- 40 MHz Crystal integrated oscillator
- Available in different versions that include 10 GHz and 5 GHz dividers
- Also includes buffers for voltage outputs at 5 GHz and 2.4 GHz
- Designed for 802.11/a/b/g applications but also suitable for other applications
- Long line driving capability (2.3 mm) @10 GHz
- Low Phase Noise (-101 dBc/Hz at 10 MHz offset)
- Fast lock: 30 micro s typical, 100 micro s max
- Fine-tuning resolution: 9.76 kHz step @ 10 GHz, 4.88 kHz step @ 5 GHz, 2.44 kHz @ 2.4 GHz
- 1 ppm accuracy
- Programmable charge pump current levels: from 400 microA to 1.8 mA
- Self-calibration circuitry included in RTL code, software algorithm separately available for better flexibility
- Low power supply current: 46 mA typical without LO buffers, 69 mA with LO buffers
- Power down (standby) mode
- 1.8 V Single Supply operation

2 Technology

0.18 um TSMC mixed signal technology

3 General Description

The RF Fractional-N synthesizer is designed to be used in a radio transceiver where the required quadrature signals are obtained via frequency division in divide-by-2 circuits included in Tx and Rx channels. This frequency division approach has the advantage of isolating the VCO from any pushing/pulling effects caused by the Power Amplifier (PA) and avoids routing of quadrature signals through the chip.

The synthesizer offers 1 ppm accuracy which gives a better EVM for critical transmission up to 54 Mb/s (for Wireless LAN application). It also allows frequency compensation of the reference crystal without manual tuning, and/or to accommodate a cheaper crystal. Programmable charge pump current levels allow to keep a constant loop bandwidth when a reference frequency different from 40 MHz is chosen.

4 Block Diagram

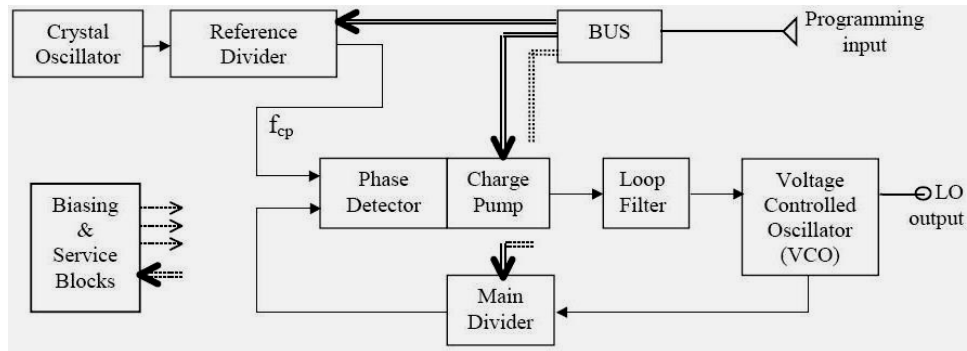


Figure 1: Functional Block Diagram

5 Application Notes

5.1 Crystal Oscillator

The internally integrated crystal oscillator runs at the recommended frequency of 40 MHz. An external crystal connected oscillates in fundamental mode, parallel resonance. External capacitors (parallel on each pin) determine frequency centering.

5.2 PAD Ring

The PLL performances can be seriously degraded by a top layout which is not carefully done resulting in possible spurs, self oscillations, and high noise. In order to ensure correct operation of the PLL, it is recommended that delivered GDSII includes Wipro-NewLogic PADs. This is a separate IP from Wipro-NewLogic.

6 Deliverables

- GDSII with/without PADs and with/without LO driver
- Basic AHDL Simulation models
- Datasheet

7 Applications

- Wireless applications including UWB, BT, WLAN, GPS
- Cable Modems, Pagers, Tester equipments
- Clock Generation

For more details about our products and services, please contact us at semi.ip@wipro.com.

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