

1.8 V 250 MHz LVDS Driver

1 Features

- 1.8V single supply operation
- Switching rate : Up to 250Mhz
- High impedance outputs in power down mode
- Low (+/- 200mV differential swing) or high (+/- 400mV differential swing) current mode controlled digitally
- Driver enable time and disable time of 10ns
- Separate biasing circuit including bandgap circuit, reference current and voltage generator

2 Technology

TSMC 0.18um CMOS Process

3 General Description

This IP core is a LVDS driver (also called Transmitter) specified to operate from a single supply between 1.8 V and 2.0 V

The LVDS driver can be set digitally to work in a low or high current mode depending on the type and the length of the load connected.

The LVDS driver comes with a separate biasing block. This biasing circuit includes a bandgap circuit, a reference current and voltage generator and a DC replica of the LVDS driver. It can bias up to 3 LVDS drivers and 3 LVDS receivers on the same chip

The LVDS Driver and biasing circuits can be placed in power down mode to reduce the power consumption.

4 Block Diagram

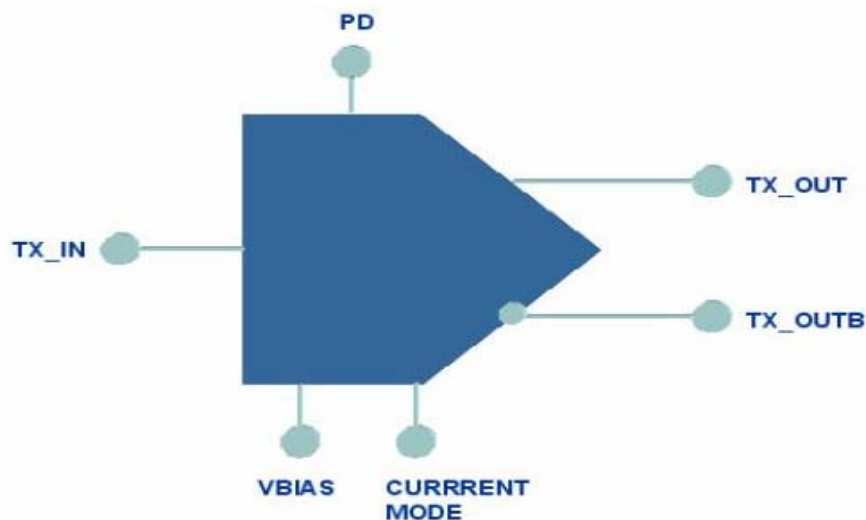


Figure 1: Functional Block Diagram



5 Deliverables

- GDSII
- Basic AHDL Simulation models
- Datasheet
- Application Note and Test Guidelines

6 Applications

- Wireless applications - Bluetooth, WLAN
- Wired applications - Serial ATA, Spacewire.
- Video, Imaging applications - digital camera interface, LCD display interface

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