

ADC – 8 bit 60 MHz

1 Features

- Resolution: 8 bits
- 1.6-2V single supply operation
- Excellent I/Q phase and gain matching
- Differential input range: -0.55v to +0.55v
- Sample rates up to 60Mhz
- Low current consumption: 30mA typical
- Power down and sleep mode
- Fast Wake up time (400ns)
- 0-9db, 3 db steps programmable gain
- 50db SNR, -50db THD over 8.3 MHz bandwidth
- Standard digital CMOS process

2 Technology

TSMC 0.18 um LOGIC 1P/6M CNL018G
TSMC 0.18um 1P/6M RFCMOS process

3 General Description

The dual 8 bit 60 MHz ADC are specifically designed with excellent phase and gain matching. A three stage pipeline architecture (4-3-3) is used for compact layout and low I/Q mismatches.

The highly critical timing requirements for applications based on 802.11a/g are supported by fast conversion and wake up time. Two alternative low power modes are provided.

Also incorporated is a power down mode where overall power consumption is less than 1microA and a sleep mode that allows faster wake up time.

The blocks were designed for low power/low voltage operation. Regulated clock boosters are used for switched capacitor sections.

For better yields and portability, no analog options are necessary.

4 Block Diagram

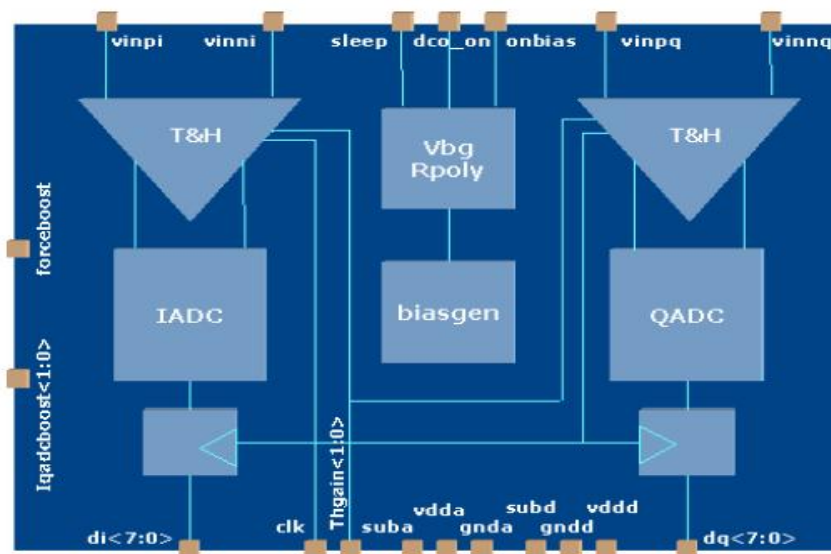


Figure 1: Functional Block Diagram

5 Deliverables

- GDSII
- Basic AHDL Simulation models
- Datasheets
- Application Note and Test Guidelines

6 Applications

- Suitable for 802.11 applications
- Bluetooth
- Software defined radio
- GSM
- DVB-H/DVB-T

7 Electrical Characterization

	Conditions	Min	Typ	Max	Units
RESOLUTION			8		Bits
DC ACCURACY					
Integral Nonlinearity (INL)		-1.0		1.0	LSB
Differential Nonlinearity (DNL)		-0.5		0.5	LSB
DC offset		-15		15	mV
Gain error		-0.5		0.5	dB
ANALOG INPUT					
Differential Input Range	0 dB gain	1.05		1.15	V _{pp}
Input Common Mode Voltage range		0.3	0.5	0.7	V
DYNAMIC PERFORMANCE					
Signal to Noise ratio	(1)		50		dB
Total harmonic distortion	(2)			-50	dB
I/Q PERFORMANCE					
I/Q gain matching	@ 8.3 Mhz	-0.15	0	0.15	dB
I/Q phase matching		-0.5	0	0.5	°
I/Q isolation			-60		dB
POWER SUPPLIES					
Analog Supply Voltage (vdda)		1.62	1.8	1.98	V
Digital Supply Voltage (vddd)		1.62	1.8	1.98	V
DC Supply Current, vdda		21	30	39	mA
DC Supply Current, vdda	Sleep	0.9	1.35	1.75	mA
DC Supply Current, vdda	Power down			1uA	
DC Supply Current, vddd	60Mhz clock			2	mA
TIMING SPECIFICATIONS					
Clock period			16.66		ns
Clock duty cycle		45		55	%
Startup time				1.2	us
Wake up time				400	ns
Data Latency (Pipeline delay)		5	5	5	Tclk

⁽¹⁾ 2 Mhz full scale sine wave, 8.3Mhz integration bandwidth, 0dB gain, 60Mhz sampling clock

⁽²⁾ 2Mhz, 0.8° Full scale sine wave inputs, 0dB gain, 60Mhz sampling clock

temperature range: -40 - 100°C, worst case V_{dd} & process otherwise noted, voltage signals are differential

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